depositing a photoresist layer on the insulation layer;

exposing and developing the photoresist layer for providing a photoresist mask pattern for subsequent etching of the insulation layer; and

removing the fill-in material from the aperture.

11. (Once Amended) In an integrated circuit manufactured using a via-first dual damascene process and having a low-K dielectric material as an insulation layer on a wafer substrate, a photolithographic pattern comprising:

an aperture etched into an insulation layer on a wafer substrate filled with a fill-in material for isolating the insulation layer from photoresist deposited thereafter; and

a photoresist layer deposited on the insulation layer, in which the photoresist layer is exposed and developed for providing a photoresist mask pattern for subsequent etching of the insulation layer

wherein the fill-in material is removed after the photoresist mask pattern is formed.

12. (Once Amended) The pattern as in claim 11, wherein the aperture is fully filled and thereafter removed.

16. (Once Amended) The pattern as in claim 11, wherein the aperture is partially filled and thereafter removed.

A marked up version of the amended claims, showing the changes by underlining of the added text and bracketing of the deleted text, is appended hereto.